



Revision Change Notice **#1410291**

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PCN Date: 10/29/2014		Effective Date: 2/4/2015	
Title: C8051F98x/9x Revision C			
Originator: Greg Hodgson		Phone: 512-532-5766	Dept: MCU & Wireless
Customer Contact: Kathy Hagggar		Phone: 512-532-5261	Dept: Sales
PCN Type: ☐ Datasheet ☒ Product Revision			
PCN Details			
Description of Change: Silicon Labs is pleased to announce hardware revision C of the C8051F98x/F99x devices and revision 1.2 of the corresponding datasheet for these products, and hardware revision C of C8051F996 wafer sales and revision 1.2 of the corresponding datasheet. Hardware revision C makes the following enhancements and modifications: 1. Changes the reset value of REVID SFR and REVID C2 will read 0x02 for Revision C instead of 0x01 for Revision B. 2. Eliminates a potential issue with the RTC after a sleep wake up in some applications. This behavior could occur when VBAT falls below 1.5V and the MCU was in sleep mode for ~100ms. If the behavior occurred, the RTC would either miss a clock period or change in frequency. 3. Improves the robustness of the device during VBAT ramp time that exceeds maximum datasheet specifications. 4. Adjusts the min, typ and max VDD brownout falling voltage threshold of the power on reset from 0.4V, 0.7V, and 1.0V respectively to 0.75V, 1.0V, and 1.3V respectively. C8051F98x/9x datasheet revision 1.2 and C8051F996-C-GDI datasheet revision 1.2 updates the orderable part number to revision C along with other minor edits noted in the datasheet change notes. Two published errata and workarounds are now documented in the datasheet: 1. Address 0x0000 of XRAM On device reset, or upon waking up from Sleep mode, address 0x0000 of external memory may be overwritten by an indeterminate value. The indeterminate value is 0x00 in most situations. 2. POR Supply Monitor for supply voltages greater than 2.4 V Description: The POR Supply Monitor should not be disabled if the supply voltage is greater than 2.4 V. After the effective date of this PCN, Silicon Labs reserves the right to deliver Revision C to customer ordering Revision B. Refer to Product Identification section of this PCN for details.			

Reason for Change:

C8051F98x/9x revision C release
 C8051F98x/9x datasheet revision 1.2 release
 C8051F996 revision C wafer sales release
 C8051F996 datasheet revision 1.2 release

Impact on Form, Fit, Function, Quality, Reliability:

The following functions are impacted:

- The reset value of REVID SFR and REVID C2
- Behavior with the RTC after a Sleep wake up has been fixed
- The robustness of the device is improved during VDD ramp time that exceeds maximum datasheet specifications.
- Adjusted VDD brownout falling voltage thresholds

Product Identification:

Revision B Existing OPN	Revision C Replacement OPN	Revision B Existing OPN	Revision C Replacement OPN
C8051F980-GM	C8051F980-C-GM	C8051F980-GMR	C8051F980-C-GMR
C8051F981-GM	C8051F981-C-GM	C8051F981-GMR	C8051F981-C-GMR
C8051F982-GM	C8051F982-C-GM	C8051F982-GMR	C8051F982-C-GMR
C8051F983-GM	C8051F983-C-GM	C8051F983-GMR	C8051F983-C-GMR
C8051F985-GM	C8051F985-C-GM	C8051F985-GMR	C8051F985-C-GMR
C8051F986-GM	C8051F986-C-GM	C8051F986-GMR	C8051F986-C-GMR
C8051F986-GU	C8051F986-C-GU	C8051F986-GUR	C8051F986-C-GUR
C8051F987-GM	C8051F987-C-GM	C8051F987-GMR	C8051F987-C-GMR
C8051F987-GU	C8051F987-C-GU	C8051F987-GUR	C8051F987-C-GUR
C8051F988-GM	C8051F988-C-GM	C8051F988-GMR	C8051F988-C-GMR
C8051F988-GU	C8051F988-C-GU	C8051F988-GUR	C8051F988-C-GUR
C8051F989-GM	C8051F989-C-GM	C8051F989-GMR	C8051F989-C-GMR
C8051F989-GU	C8051F989-C-GU	C8051F989-GUR	C8051F989-C-GUR
C8051F990-GM	C8051F990-C-GM	C8051F990-GMR	C8051F990-C-GMR
C8051F991-GM	C8051F991-C-GM	C8051F991-GMR	C8051F991-C-GMR
C8051F996-GM	C8051F996-C-GM	C8051F996-GMR	C8051F996-C-GMR
C8051F996-GU	C8051F996-C-GU	C8051F996-GUR	C8051F996-C-GUR
C8051F997-GM	C8051F997-C-GM	C8051F997-GMR	C8051F997-C-GMR
C8051F997-GU	C8051F997-C-GU	C8051F997-GUR	C8051F997-C-GUR
C8051F996-GDI	C8051F996-C-GDI		

Last Date of Unchanged Product: 2/4/2015

Qualification Samples:

Samples are available now. Please contact your Silicon Labs sales representative to order samples.
 A list of Silicon Labs sales representatives is available at www.silabs.com.



Revision Change Notice #1410291

Specific conditions of acceptance of this change will be considered on a case by case basis if written notice is submitted within 30 days of this notice. To request further data or inquire about this notification, please contact your local Silicon Labs sales representative. A list of Silicon Labs sales representatives is available at www.silabs.com.

In some cases rejection of a change notice may impact Silicon Labs product pricing, delivery, quality, or reliability.

Customer Early Acceptance Sign Off:

Customers may approve early PCN acceptance by completing the information below:

Early Acceptance: Date: _____

 Name: _____

 Company: _____

Email your early Acceptance approval to: katherine.haggard@silabs.com

Qualification Data:

Qualification data is available in the Appendix.

Appendix

C8051F98x/9x Rev B and Rev C Qualification Report



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C8051F98x/9x, Rev B and Rev C, TSMC 0.18um Fabrication							
Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
Test Group A - Accelerated Environment Stress Tests - UTACTH - QSOP - CuPd Wire							
HAST	JA110 100 °C, 85%RH Vcc=3.6V, 264 hours	3 lots, N=>25	Q33781	0/27	3, 4	3 lots 0/80	Pass
			Q33784	0/27	3, 4		
			Q33769	0/26	3, 4		
Temp Cycle	JA104 Cond C: -65 °C to 150 °C 500 cycles	3 lots, N=>25	Q33783	0/30	3, 4	3 lots 0/90	Pass
			Q33780	0/30	3, 4		
			Q33767	0/30	3, 4		
HTSL	JA103 150 °C, 1000hr	3 lots, N=>25	Q33782	0/30	3	3 lots 0/90	Pass
			Q33768	0/30	3		
			Q33785	0/30	3		
Test Group A - Accelerated Environment Stress Tests - ASECL-QFN - CuPd Wire							
HAST	JA110 100 °C, 85%RH Vcc=3.6V, 264 hours	3 lots, N=>25	Q33300	0/40	1, 4	5 lots 0/200	Pass
			Q33303	0/40	1, 4		
			Q33411	0/40	2, 4		
			Q33408	0/40	2, 4		
			Q33138	0/40	2, 4		
Temp Cycle	JA104 Cond C: -65 °C to 150 °C 500 cycles	3 lots, N=>25	Q33302	0/40	1, 4	4 lots 0/149	Pass
			Q33413	0/40	2, 4		
			Q33410	0/40	2, 4		
			Q33337	0/29	2, 4		
HTSL	JA103 150 °C, 1000hr	3 lots, N=>25	Q33412	0/40	2	3 lots 0/108	Pass
			Q33409	0/40	2		
			Q33336	0/28	2		
Test Group A - Accelerated Environment Stress Tests - Unisem - 24 QSOP - Au Wire							
HAST	JA110 130 °C, 85%RH Vcc=3.6V, 96 hours	3 lots, N=>25	Q29019	0/79	3, 5	3 lots 0/234	Pass
			Q29022	0/77	3, 5		
			Q29163	0/78	3, 5		
Temp Cycle	JA104 Cond C: -65 °C to 150 °C 500 cycles	3 lots, N=>25	Q29023	0/81	3, 5	3 lots 0/199	Pass
			Q29162	0/78	3, 5		
			Q33524	0/40	3, 5		
HTSL	JA103 150 °C, 1000hr	3 lots, N=>25	Q29021	0/58	3, 5	3 lots 0/137	Pass
			Q29024	0/33	3, 5		
			Q29161	0/46	3, 5		

Approved by: K. Torres

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Prepared on: 24-Sept-2014

C8051F98x/9x Rev B and Rev C Qualification Report



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C8051F98x/9x, Rev B and Rev C, TSMC 0.18um Fabrication							
Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
Test Group A - Accelerated Environment Stress Tests - ASECL-QFN - Au Wire							
HAST	JA110 130°C, 85%RH Vcc=3.6V, 96 hours	3 lots, N=>25	Q32603 Q32600 Q32607	0/30 0/30 0/30	2, 4 2, 4 2, 4	3 lots 0/90	Pass
Temp Cycle	JA104 Cond C: -65°C to 150°C 500 cycles	3 lots, N=>25	Q32650 Q32602 Q32609	0/30 0/30 0/30	2, 4 2, 4 2, 4	3 lots 0/90	Pass
HTSL	JA103 150°C, 1000hr	3 lots, N=>25	Q32604 Q32601 Q32608	0/30 0/30 0/30	2, 4 2, 4 2, 4	3 lots 0/90	Pass
Test Group B - Accelerated Lifetime Simulation Tests							
HTOL	JA108 125°C, Dynamic Vcc=3.3V, 1000 hours	3 lots, N=>77	Q27065 Q28301 Q28955	0/88 0/80 0/80	3 1 1	3 lots 0/248	Pass
LTOL	JA108 -10°C, Dynamic Vcc=3.3V, 1000 hours	1 lot, N=>32	Q25548	0/39	2	1 lots 0/39	Pass
ELFR	JA108 125°C, Dynamic Vcc=3.3V, 48 hours	3 lots, N=>500	Q27592 Q28218 Q28868 Q29440	0/520 0/514 0/516 0/492	1 1 1 1	4 lots 0/2042	Pass
NVM Endurance, Retention and Operating Life	AEC Q100-005 25°C	3 lots, N=>38	QQ26230 QQ26233 QQ28728 QQ28730	0/40 0/40 0/156 0/156		4 lots 0/392	Pass
NVM Endurance, Retention and Operating Life	AEC Q100-005 125°C	3 lots, N=>39	QQ26231 QQ26232 QQ28727 QQ28729	0/40 0/40 0/126 0/126		4 lots 0/332	Pass

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C8051F98x/9x Rev B and Rev C Qualification Report



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C8051F98x/9x, Rev B and Rev C, TSMC 0.18um Fabrication							
Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
Test Group D - Die Fabrication Reliability Tests							
Electromigration	ASTM F1260-96	30 samples per structure	Q92446 Q92447 Q92448	0/30 0/30 0/30		3 lots 0/90	Pass
Time Dependent Dielectric Breakdown	Foundry proprietary qualification spec	2 structures * 260 samples	Q92446 Q92447 Q92448	0/260 0/260 0/260		3 lots 0/780	Pass
Hot Carrier Injection	Foundry proprietary qualification spec	10 DUTs	Q92446 Q92447 Q92448	0/10 0/10 0/10		3 lots 0/30	Pass
Negative Bias Temperature Instability	Foundry proprietary qualification spec	10 transistors per structure	Q92446 Q92447 Q92448	0/10 0/10 0/10		3 lots 0/30	Pass
Test Group E - Electrical Verification							
ESD-HBM	JA114	1 lot, N=>3	Q33027	±2.5kV	1		Pass
ESD-MM	JA115	1 lot, N=>3	Q33025	±250V	1		Pass
ESD-CDM	JC101	1 lot, N=>3	Q33026 Q33238 Q34029	±2KV ±2KV ±2KV	2 1 3		Pass
Latch Up	JESD78 ±200mA Overvoltage = 3.6V	1 lot, N=>6	Q33029 Q33028	85°C 25°C	2 2		Pass

Notes:

- 1 - 20 QFN- 3x3
- 2 - 24-TQFN-4X4-LF
- 3 - 24 QSOP
- 4 - Preceded by MSL1, 260°C Preconditioning
- 5 - Preceded by MSL2, 260°C Preconditioning

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C8051F98x/9x, Rev B and Rev C, TSMC 0.18um Fabrication

Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
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The qualification data applies to the following part numbers:

C8051F980-GM	C8051F986-GM	C8051F988-GU	C8051F996-GM
C8051F981-GM	C8051F986-GU	C8051F989-GM	C8051F996-GU
C8051F982-GM	C8051F987-GM	C8051F989-GU	C8051F997-GM
C8051F983-GM	C8051F987-GU	C8051F990-GM	C8051F997-GU
C8051F985-GM	C8051F988-GM	C8051F991-GM	C8051F996-GDI
C8051F980-C-GM	C8051F986-C-GM	C8051F988-C-GU	C8051F996-C-GM
C8051F981-C-GM	C8051F986-C-GU	C8051F989-C-GM	C8051F996-C-GU
C8051F982-C-GM	C8051F987-C-GM	C8051F989-C-GU	C8051F997-C-GM
C8051F983-C-GM	C8051F987-C-GU	C8051F990-C-GM	C8051F997-C-GU
C8051F985-C-GM	C8051F988-C-GM	C8051F991-C-GM	C8051F996-C-GDI

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